QUASI-STATIC APPROACH TO SIMULATING NONLINEAR GaAs FET BEHAVIOR

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ABSTRACT

A technique is described for accurately predicting nonlinear performance of microwave GaAs field-effect transistors in arbitrary circuit embedding using a quasi-static device model. Excellent agreement with experimental results at X-band is demonstrated.

Introduction

Current interest is focusing on fundamental aspects of nonlinear GaAs FET performance to establish the basis for improved circuit designs. Investigations have so far been predominantly empirical, relying on linear circuit considerations and simplified models for guidelines. In many instances, acceptable results can be achieved in this way; but they are often burdened with the uncertainty of not having fully exploited device performance capabilities. Better control over nonlinear device-circuit interaction can be gained in the design stage, of course, by working directly from sufficient large-signal experimental data on the device. The accuracy in assessing this interaction can, however, become impractical due to the amount of data that has to be assimilated--especially when wide frequency ranges and wide dynamic ranges are involved simultaneously.

The model described here condenses all necessary information relevant to device nonlinear behavior into a concise and manageable format. One of the main attributes of the present approach is that it enables the model to be derived solely from small-signal device characteristics and their bias voltage dependence. No direct measurements of nonlinear device performance (power gain, intermodulation, etc.) are required to fully define the model. Excellent agreement is demonstrated between measured and model-predicted power gain characteristics of a GaAs FET terminated in arbitrary loads, complementing results reported earlier.[1,2]

The Method

The generalized technique presented here for simulating nonlinear performance of a GaAs FET is based on a circuit-type model whose topology is shown in Fig.1. The model consists of linear and nonlinear circuit elements. Values for both types of elements are determined from small-signal device S-parameters, measured as functions of gate-to-source bias voltage, V_{GS}, drain-to-source bias voltage, V_{DS}, and frequency. The element values are found by first fitting, for one discrete bias condition at a time, a small-signal model (with the same topology as in Fig.1) to the experimental data. The elements with essentially bias-independent values are considered linear. The remaining elements are the nonlinear ones. The derivation of their current-voltage relationships, based on the bias dependence of their small-signal values, is outlined in the following.

For the specific device from Texas Instruments, Inc.(1.7μm gate length, 600μm gate width) considered here, the six elements C_{IN}, C_{FB}, G_{IN}, G_{GD}, G_M and G_O comprise the major nonlinearities. The small-signal current-voltage relationships for each of these elements is written in the form

$$\tilde{i}_G(t) = \tilde{G}(V_1,V_2) \cdot \tilde{v}_G(t) \tag{1}$$

$$\tilde{i}_C(t) = \tilde{C}(V_1,V_2) \cdot \frac{d\tilde{v}_C(t)}{dt} \tag{2}$$

whereby "G" refers symbolically to any one of the conductance-type elements and "C" to either one of the capacitive nonlinearities. The tilde is used systematically through this discussion to designate all small-signal quantities. In equations (1) and (2), $\tilde{G}$ and $\tilde{C}$ are both assumed to be functions of the static internal voltages V_1 and V_2 defined in Fig.1. By accounting for the static voltage drops across the parasitic resistances, the functions are readily obtained from the experimentally determined dependences of the small-signal element values on the external bias voltages, V_{GS} and V_{DS}. Furthermore, the fact that the state of thermal equilibrium in the device is different for each bias condition has to be taken into consideration.

Analogous to the small-signal case, the instantaneous (large-signal) current-voltage relationship for each nonlinear element is written as:

$$\hat{i}_G(t) = \hat{G}[\hat{v}_1(t), \hat{v}_2(t)] \cdot \hat{v}_G(t) \tag{3}$$

$$\hat{i}_C(t) = \hat{C}[\hat{v}_1(t), \hat{v}_2(t)] \cdot \frac{d\hat{v}_C(t)}{dt} \tag{4}$$

The hat is used to designate an instantaneous quantity. The instantaneous element values $\hat{G}$ and $\hat{C}$ are expressed in terms of the two (now time-varying)voltages $\hat{v}_1(t)$ and $\hat{v}_2(t)$. It should be noted that the expressions do not include an explicit time dependence and are thus termed "time-invariant."[3] The postulate that the model elements be time-invariant is fundamental to the approach described here. The justification for this postulate is based on the physical structure of a typical microwave GaAs FET and its operation as a majority carrier device. As has been verified experimentally at least up thru X-band, the time-invariance postulate does, indeed, provide a very powerful working assumption. Substantial evidence thereof has already been given in References 1 and 2. Other investigations reported in the recent literature[4-6] also support the validity of the time-invariance assumption--at least as far as its applicability to small-signal conditions is concerned. Additional supporting evidence will be given in this paper.

To determine the unknown instantaneous element expressions in equations (3) and (4), the same test conditions are applied to the device model as were applied previously to the device itself when measuring its bias-dependent small-signal characteristics. Under these conditions each current and voltage associated with a particular nonlinear model element may be decomposed into a static and a small-signal dynamic component. From equations (3) and (4), first-order perturbation expressions for the small-signal currents thru each of the nonlinear elements are derived. Using the previous symbol definitions and capital V's to describe static voltages, it follows for conductance-type elements

$$\tilde{i}_G(t) = \left\{ \hat{G}(v_1,v_2) \cdot \tilde{v}_G(t) + V_G \cdot \frac{\partial \hat{G}(v_1,v_2)}{\partial v_1} \cdot \tilde{v}_1(t) \right.$$
$$\left. + V_G \cdot \frac{\partial \hat{G}(v_1,v_2)}{\partial v_2} \cdot \tilde{v}_2(t) \right|_{v_1=V_1, \ v_2=V_2} \right\} \tag{5}$$

and for capacitance-type elements

$$\tilde{I}_C(t) = \left\{ \hat{C}(v_1, v_2) \cdot \frac{d\tilde{v}_C(t)}{dt} \bigg|_{v_1 = V_1, \ v_2 = V_2} \right\} \quad (6)$$

Thru the equivalence of relationships (1) and (5) as well as (2) and (6), partial differential equations in the instantaneous quantities are obtained. Based on these equations the instantaneous element expressions can be derived in terms of the experimentally determined small-signal values. This leads to

$$\hat{C}_{IN}(V_1, V_2) = \tilde{C}_{IN}(V_1, V_2) \quad (7)$$

$$\hat{C}_{FB}(V_1, V_2) = \tilde{C}_{FB}(V_1, V_2) \quad (8)$$

$$\hat{G}_{IN}(V_1, V_2) = \tilde{G}_{IN}(V_1, V_2) \quad (9)$$

$$\hat{G}_{GD}(V_1, V_{GD}) = \frac{1}{V_{GD}} \int_0^{V_{GD}} \tilde{G}_{GD}(V_1, v) \, dv \quad (10)$$

Note that in equation (10) the voltage V_{GD} across G_{GD} (Fig.1) has been substituted for V_2. Instead of similarly defining an instantaneous transconductance and an instantaneous output conductance, the current i_{GOM} thru the parallel combination of the two elements is calculated directly. In terms of static voltages V_1 and V_2, referenced to their quiescent values, the static current

$$I_{GOM}(V_1, V_2) = V_1 \cdot \overline{G}_M(V_1, V_2) + V_2 \cdot \overline{G}_O(0, V_2)$$
$$= V_1 \cdot \overline{G}_M(V_1, 0) + V_2 \cdot \overline{G}_O(V_1, V_2) \quad (11)$$

is obtained with

$$\overline{G}_M(V_1, V_2) = \frac{1}{V_1} \int_0^{V_1} \tilde{G}_M(v, V_2) \, dv \quad (12)$$

$$\overline{G}_O(V_1, V_2) = \frac{1}{V_2} \int_0^{V_2} \tilde{G}_O(V_1, v) \, dv \quad (13)$$

The two solutions indicated in equation (11) are equally valid; they differ only because of inaccuracies introduced thru the measured small-signal quantities and thru the model itself. (The mean value of the two solutions is typically used to smooth out the minor discrepancies.)

The crux of the approach is that--even though the relationships (7) thru (13) have been derived under static conditions--the expressions remain equally valid when dynamic voltages are substituted for the static ones. This is a direct consequence of the postulate that the model elements be time-invariant. Because the relationships are initially established in terms of static voltages, the approach is called "quasi-static."

Experimental Verification

The relationships (7) thru (13) define the quasi-static FET-model which is directly compatible with time-domain analysis. To validate the approach, the technique has been applied to the 1.7μmX600μm device. The extensive characterization of this device reported in Reference 1 provided the basis for determining the instantaneous quantities via equations (7) thru (13). As an illustration, the total current I_{GOM} thru the parallel combination of the drain-to-source current generator and output conductance is plotted in Fig.2 as a function of V_1 and V_2, normalized to the quiescent operating point. The current was calculated by averaging the two result of equation (11). Both

results were, however, already in very close agreement (typically within ±3mA). The static I_{DS}-V_{DS} characteristics of the device are given in Fig.3 for comparison with the intrinsic "dynamic" characteristics of Fig.2. The differences between the general shapes of the two sets of curves are partly attributed to the presence of thermal and Gunn domain effects in the static case, whereas these effects are excluded in the dynamic case.

The quasi-static technique was employed to predict power gain as a function of complex load impedance presented to the drain-to-source port of the device. Fig. 4 illustrates the excellent agreement obtained between model predictions and experimental "load-pull" characteristics. For this test the device was driven at 8.5 GHz from a 50Ω source with an incident power level of +20 dBm. At this power level, the FET is operating at about 3 dB of gain compression when the load impedance is set for maximum small-signal gain. This can be seen by comparing the large-signal curves with the small-signal constant gain contours depicted in Fig.5. The measured and predicted small-signal contours virtually coincide so that only one set of curves has been plotted.

Applications

The quasi-static technique has been successfully employed for simulating in the time domain both FET power amplifiers and FET oscillators. The model can, however, easily be reformulated for direct application in frequency-domain problems, such as in the design of amplifiers for low harmonic and intermodulation distortion.

Based on the demonstrated reliability in predicting nonlinear device behavior for arbitrary complex load-conditions, the model provides, in particular, a very powerful instrument for amplifier design. The technique will prove especially useful for seeking optimum tradeoffs among distortion characteristics, efficiency, large-signal gain, and small-signal gain. The model as derived directly from laboratory measurements most accurately describes performance of a given device. The versatility of the quasi-static technique can be further enhanced by pairing it with the results of recent analytical modeling efforts. Although the approximate analytical solutions don't provide the required accuracy by themselves, these solutions can be used to assess effects on performance due to perturbations of device structure and material parameters.

Conclusions

In conjunction with work reported earlier, the technique presented here has been demonstrated to be capable of accurately simulating nonlinear performance of a GaAs FET in an arbitrary circuit environment up thru at least X-band. Among the attractive features of this technique is that its implementation requires only small-signal information on the device, thus avoiding the necessity to perform direct measurements of device nonlinear characteristics.

References

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2. B.Sheleg,C.Rauscher,H.A.Willing, & W.H.Ku,"Techniques for design, test & evaluation of GaAs FET components for phased array applications," Proc.1978 Military Microwave Conf.(London),pp.117-123, Oct.1978.
3. L.O.Chua,"Introduction to nonlinear network theory," McGraw-Hill, New York, 1969.
4. R.A.Minasian,"Large-signal GaAs MESFET model & distortion analysis,"Electronic Letters,Vol.14,pp.183-185, Mar.1978.
5. R.A.Minasian,"Analysis of intermodulation distortion in GaAs MESFET amplifiers,"Electronic Letters, Vol.14, pp.590-591, Aug.1978.

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termodulation distortion properties of a GaAs FET,"
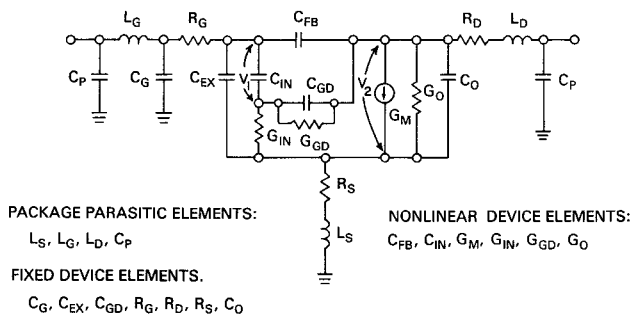Electronic Letters, Vol.13, pp.508-510, Aug.1977.

PACKAGE PARASITIC ELEMENTS:

L_S, L_G, L_D, C_P

FIXED DEVICE ELEMENTS.

C_G, C_{EX}, C_{GD}, R_G, R_D, R_S, C_O

NONLINEAR DEVICE ELEMENTS:

C_{FB}, C_{IN}, G_M, G_{IN}, G_{GD}, G_O

FIGURE 1: NONLINEAR CIRCUIT-TYPE MODEL OF A
MICROWAVE GaAs FET.
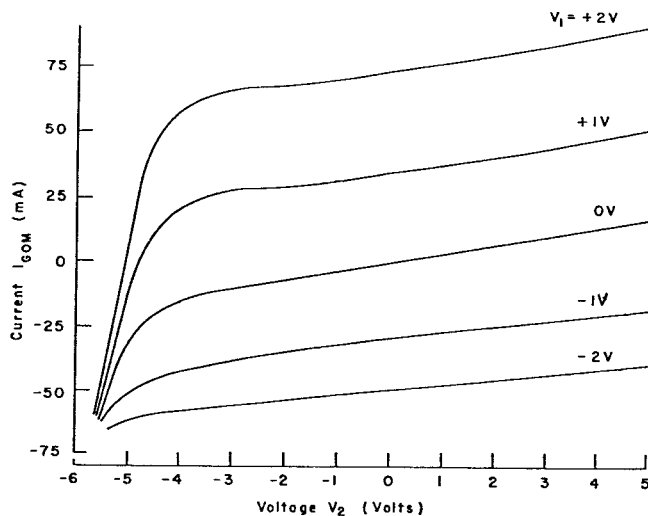
FIGURE 2: CALCULATED CURRENT I_{GOM} FOR MODELED
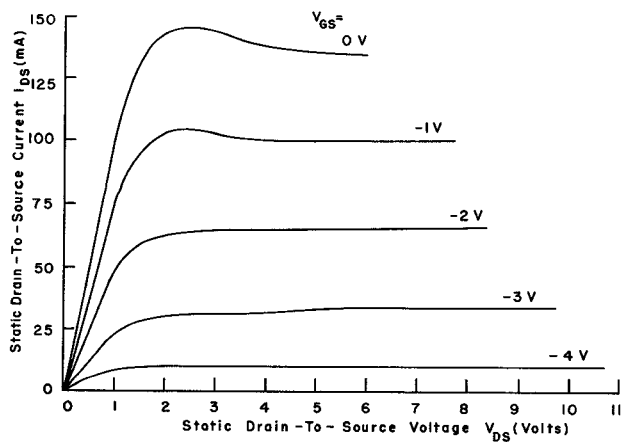1.7μm×600μm DEVICE BIASED AT V_{GS} =
-2V, V_{DS} = +6V

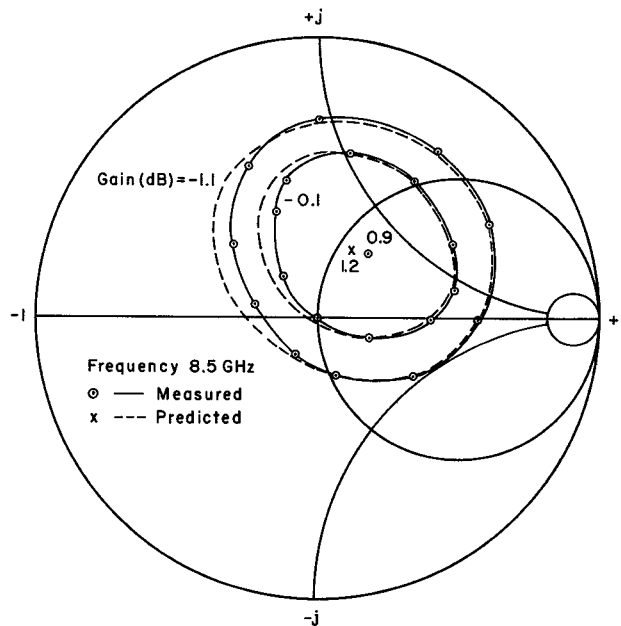FIGURE 3: MEASURED STATIC I_{DS}-V_{DS} CURVES.

FIGURE 4: CONTOURS OF CONSTANT POWER GAIN AT
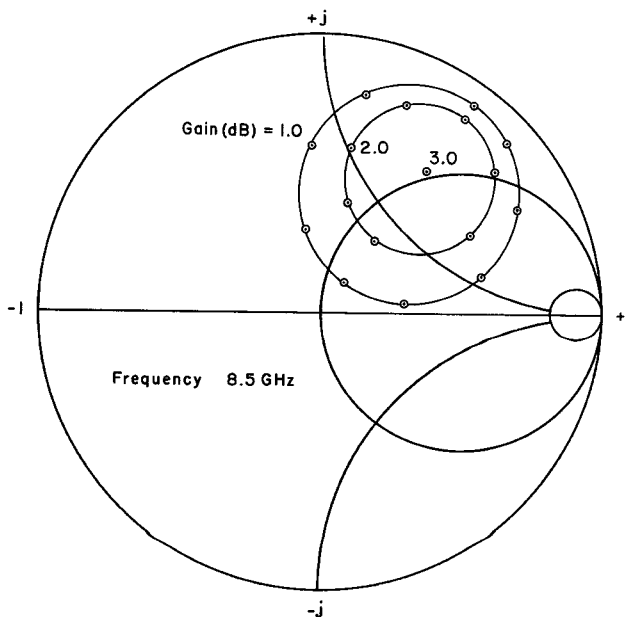8.5 GHz PLOTTED IN THE OUTPUT LOAD RE-
FLECTION PLANE.

FIGURE 5: SMALL-SIGNAL CONSTANT GAIN CONTOURS AT
8.5 GHz PLOTTED IN THE OUTPUT LOAD RE-
FLECTION PLANE.